REMARKS

Reconsideration is respectfully requested.

Claims 1-9 are pending in this application. Claims 1, 8 and 9 are amended. New claims 10-19 are presented.

The Examiner notes that formal drawings will be required when the application is allowed. Applicant will submit formal drawings at that time. The Examiner also states that this application was filed under former 37 C.F.R. §1.60. Applicant is not aware of any filing under 37 C.F.R. §1.60 relative to this application. However, if the Examiner believes that there was a filing under 37 C.F.R. §1.60, please contact the undersigned attorney, as we would like to resolve this point.

Claims 1 and 4-8 rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Masterson et al (U.S. 5,073,851). Applicant respectfully traverses. The Examiner refers to Masterson et al column 5, lines 57-60, as teaching a read to a first destination "substantially simultaneously overlapped" with a write of a second destination. What Masterson et al discuss here is a different concept from that to which applicant's claimed invention pertains. In the cited portion of Masterson et al, a read of data byte #2 is taking place at about the same time that a write of data byte #1 is happening. This is not what applicant claims. Applicant's invention relates to supplying the same data substantially simultaneously to two different devices. One of those devices is accessing the data as a read operation, while the other is accessing the data as a write operation. If the



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style of description of Masterson et al is applied to applicant's situation, then one would say that data byte 1 from MAC 14 is being read by the DSP 20 substantially simultaneously with data byte 1 being written to the SDRAM 18. This all occurs on BUS 16. Masterson et al do not appreciate this concept, and are concerned with something different entirely. Therefore, the claimed invention would not be obvious in view of Masterson et al, because Masterson et al are not addressing the issues applicant is.

Applicant is concerned with being able to rapidly provide data from a non-addressed device such as a FIFO to more than one addressed device such as memory and a processor. Applicant's invention accomplishes this rapidly, as in applicant's operating environment, data is transferring at gigabit rates. Were applicant to follow prior art processes of transferring the data on the bus to the processor from the FIFO device, and then, if the processor determines that the data should be stored to memory, transferring the data from the processor to memory, too much time will have passed to accommodate the gigabit data rates. Therefore, applicant has devised the claimed devices and methods.

Claim 1 is amended to clarify the distinction, that the data being read and written is a discrete unit of data. That is, unlike Masterson, which is discussing reading a second byte while a first byte is being written, applicant is simultaneously reading a given quantity of data to one device and writing that given quantity of data to another device. Claim 8 is amended to clarify that selected ones of discrete units of data are written



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substantially simultaneously. Thus a given bit or byte or word of data is written to one device while being read into the other device in simultaneous fashion. This contrasts with Masterson et al, which teach writing one particular unit of data while a different distinct unit of data is being read.

Claims 1 and 8 are submitted to be allowable in view of the above comments and remarks, as Masterson et al do not appreciate the problem which applicant is addressing, and are not concerned with the same concepts and issues that applicant is addressing. Therefore, combining AAPA with Masterson et al would not teach or suggest applicant's claims. Also, claims 4-7, which depend from claim 1, are also submitted to be allowable.

Claims 2, 3 and 9 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over AAPA in view of Masterson et al (U.S. 5,073,851) as applied to claims 1 and 4-8 above, and further in view of DeSousa (U.S. 5,279,389). Applicant respectfully traverses.

For reasons corresponding to those noted above with regard to claims 1 and 4-8, Masterson et al in combination with AAPA does not teach or suggest the claimed invention of claims 2, 3 and 9. DeSousa does not add any further teaching or suggestions which would result in applicant's claims. Claim 9 is amended to clarify this distinction of a selected quantity of data being simultaneously processed in the claimed manner. This is not taught or suggested by DeSousa, nor by Masterson, nor by AAPA, nor by the combination of these. Claims 2 and 3 are also



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submitted to be allowable as depending on claim 1, which as noted above is allowable.

New claims 10-19 are presented here. Claim 10 depends on 9 and adds that said FIFO device is a media access controller. Claim 13 depends on claim 2, adding that the source comprises a media access controller device. Support for this is found in the specification as filed, at page 2, lines 28-30. Claim 11 also depends on claim 9, and adds that said FIFO device is a media access controller and that the apparatus is a network test instrument. Claim 14 depends on claim 8, adding the concept of a network test instrument. Support is found for the device and method in a network test instrument at page 2, lines 15-16 and 28-30.

Claim 12 depends on claim 1, adding that said supplying as a read and write operation of said unit of data is accomplished with said unit of data being presented on said bus as a single instance. Claim 15 depends on claim 8, adding corresponding language. Claim 16 is a new independent claim including the concept of said step of supplying data to said processor and said step of supplying data to said memory are accomplished substantially simultaneously with use of the same transfer of said data on said bus. These claims are supported by FIG. 2 as filed, which is a timing diagram of operation according to the invention, and the accompanying description.

Claim 17 depends on claim 16, adding steps related to determining whether data is to be kept in memory or discarded, and how the next data write location is handled based on that



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determination. Claim 18 adds a corresponding concept to claim 1 Support for the language of these claims is found at page 5, lines 19-28 of the specification.

Claim 19 adds that the unit of data in claim 1 is a word. Support for this concept is found in the specification as filed at page 4, line 32, for example.

New claims 10-19 are respectfully submitted to be allowable.

The other documents made of record in the action, but not relied on, have been considered, and it is respectfully submitted that they are not relevant in view of the above remarks.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.



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In light of the above noted amendments and remarks, this application is believed in condition for allowance and notice thereof is respectfully solicited. The Examiner is asked to contact applicant's attorney at 503-224-0115 if there are any questions.

Respectfully submitted,

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